PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-273376
(43)Date of publication of application : 18.10.1996

(51)Int.Cl. G11C 15/04

(21)Application number : 07-074034
(22)Date of filing : 30.03.1995

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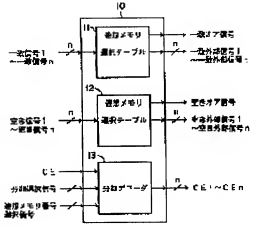
(54) ASSOCIATIVE MEMORY SYSTEM

(57)Abstract:

PURPOSE: To provide an associative memory system in which a plurality of associative memories can be accessed freely for each group by providing a controller for bringing an associative memory, belonging to a desired group in the plurality of associative memories, into chip enable state.

CONSTITUTION: An associative memory controller 10 comprises an associate memory selection table 11 for coincidence signal, 2 an associate memory selection table 12 for blank signal, and a sorting decoder 13. The table 11 receives coincidence signals 1-n from (n) associate memories and delivers coincidence external signals 1-n and a coincidence OR signal. The sorting decoder 13 receives a chip enable signal CE, a sort selection signal and an associate memory number selection signal to produce a chip enable signal CE1-CEn for each associate memory.



LEGAL STATUS

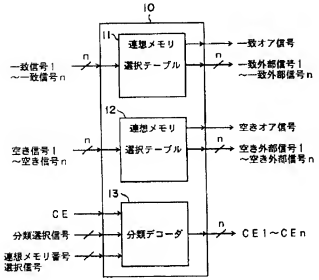
[Date of request for examination] 09.01.2002

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

Drawing selection Representative drawing



[Translation done.]

[Patent number]	3703518
[Date of registration]	29.07.2005
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, in the associative memory system equipped with two or more associative memories, the associative memory of these plurality is classified into plurality, and the associative memory of these plurality can be freely accessed for every classification.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, in the system using two or more associative memories, two or more associative memories used for the system are classified into plurality, and there is a case where he wants to access for every classification. However, although the method indicated by above-mentioned JP,3-52160,B is suitable for dealing with it in two or more associative memories by which cascade connection was carried out as if it was one associative memory with big memory space, it cannot access the associative memory of these plurality for every classification.
[0007] Moreover, although the associative memory which it had can be independently accessed with the technique proposed by above-mentioned JP,6-251589,B, since it is dependent on data, assignment of the associative memory accessed cannot access a desired associative memory freely. In view of the above-mentioned situation, this invention classifies the associative memory of these plurality into plurality, when it has two or more associative memories, and it aims at offering the associative memory system which can access the associative memory of these plurality freely for every classification.

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PRIOR ART

[Description of the Prior Art] In recent years, the associative memory is widely used for fields with the need of performing high-speed search, such as a communicative field. Drawing 10 is a circuit block diagram showing an example of an associative memory. This associative memory 100 is equipped with many memory areas 111a, 111b, --, 111k which consist of two or more memory cells on a par with the longitudinal direction of drawing. Moreover, all of the retrieval data which this associative memory 100 was equipped with the retrieval register 112 which retrieval data are inputted and is latched, and were latched to the retrieval register 112, or some [predetermined] bit patterns, The inside of the data indicated in each memory areas 111a, 111b, --, 111k, The coincidence inequality of the above-mentioned bit pattern and the corresponding bit pattern of a part is compared. It corresponds to each of each memory areas 111a, 111b, --, 111k. The coincidence signal of logic '1' is outputted to the coincidence lines 114a, 114b, --, 114k corresponding to the memory areas 111a, 111b, --, 111k whose bit patterns corresponded among the coincidence lines 114a, 114b, --, 114k which it had. The inequality signal of logic '0' is outputted to the other coincidence lines 114a, 114b, --, 114k.

[0003] Here, '0', '1', '0', '0', '1', --, the signal of '0' should be outputted to each flag lines 114a, 114b, --, 114k, respectively. This signal is inputted into a priority encoder 115, and address signal AD corresponding to the coincidence line of highest top priority of the priority of the coincidence lines (here, it is two, coincidence line 114b and coincidence line 114e) by which the coincidence signal of logic '1' was outputted is outputted from this priority encoder 115. Here, it considers as what has high priority, so that the alphabet of a subscript is young, therefore coincidence line 114b becomes a coincidence line of the highest priority. Address signal AD corresponding to coincidence line 114b of the highest priority outputted from this priority encoder 115 is inputted into the address recorder 116 if needed. By the address recorder 116, an access signal (here signal of logic '1') is outputted to any one word line (here word line 117b) corresponding to address signal AD into which it was inputted of the word lines 117a, 117b, --, 117k which decoded this inputted address signal AD and it had corresponding to each of each memory areas 111a, 111b, --, 111k. The data memorized by memory WORD 111b corresponding to word line 117b to which the access signal was outputted by this are read to an output register 118.

[0004] An associative memory 100 is the memory which can search the contents (data) memorized in many memory areas 111a, 111b, --, 111k using retrieval data, and can read the whole data which obtained the address of the memory area where data in agreement were memorized, and was memorized in the memory area as mentioned above. In the system using the above associative memories, by one associative memory, when memory space runs short, two or more associative memories will be used.

[0005] The technique of dealing with two or more associative memories as if it was one associative memory with big memory space is proposed by JP,3-52160,B about the system using two or more associative memories by carrying out cascade connection of two or more associative memories. Moreover, it stands in a row in JP,6-251589,A, two or more associative memories are prepared in it, the associative memory set as the object of retrieval of data and storage by sorting out the associative memory which makes the data memorize beforehand according to data is specified, and the technique which shortens the time amount which retrieval and storage take by this is indicated.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The field of the invention on difference industry] This invention relates to the associative memory system which used two or more associative memories.
[0002]
[Description of the Prior Art] In recent years, the associative memory is widely used for fields with the need of performing high-speed search, such as a communicative field. Drawing 10 is a circuit block diagram showing an example of an associative memory. This associative memory 100 is equipped with many memory areas 111a, 111b, --, 111k which consist of two or more memory cells on a par with the longitudinal direction of drawing. Moreover, all of the retrieval data which this associative memory 100 was equipped with the retrieval register 112 which retrieval data are inputted and is latched, and were latched to the retrieval register 112, or some [predetermined] bit patterns, The inside of the data indicated in each memory areas 111a, 111b, --, 111k, The coincidence inequality of the above-mentioned bit pattern and the corresponding bit pattern of a part is compared. It corresponds to each of each memory areas 111a, 111b, --, 111k. The coincidence signal of logic '1' is outputted to the coincidence lines 114a, 114b, --, 114k corresponding to the memory areas 111a, 111b, --, 111k whose bit patterns corresponded among the coincidence lines 114a, 114b, --, 114k which it had. The inequality signal of logic '0' is outputted to the other coincidence lines 114a, 114b, --, 114k.
[0003] Here, '0', '1', '0', '0', '1', --, the signal of '0' should be outputted to each flag lines 114a, 114b, --, 114k, respectively. This signal is inputted into a priority encoder 115, and address signal AD corresponding to the coincidence line of highest top priority of the priority of the coincidence lines (here, it is two, coincidence line 114b and coincidence line 114e) by which the coincidence signal of logic '1' was outputted is outputted from this priority encoder 115. Here, it considers as what has high priority, so that the alphabet of a subscript is young, therefore coincidence line 114b becomes a coincidence line of the highest priority. Address signal AD corresponding to coincidence line 114b of the highest priority outputted from this priority encoder 115 is inputted into the address recorder 116 if needed. By the address recorder 116, an access signal (here signal of logic '1') is outputted to any one word line (here word line 117b) corresponding to address signal AD into which it was inputted of the word lines 117a, 117b, --, 117k which decoded this inputted address signal AD and it had corresponding to each of each memory areas 111a, 111b, --, 111k. The data memorized by memory WORD 111b corresponding to word line 117b to which the access signal was outputted by this are read to an output register 118.
[0004] An associative memory 100 is the memory which can search the contents (data) memorized in many memory areas 111a, 111b, --, 111k using retrieval data, and can read the whole data which obtained the address of the memory area where data in agreement were memorized, and was memorized in the memory area as mentioned above. In the system using the above associative memories, by one associative memory, when memory space runs short, two or more associative memories will be used.
[0005] The technique of dealing with two or more associative memories as if it was one associative memory with big memory space is proposed by JP,3-52160,B about the system using two or more associative memories by carrying out cascade connection of two or more associative memories. Moreover, it stands in a row in JP,6-251589,A, two or more associative memories are prepared in it, the associative memory set as the object of retrieval of data and storage by sorting out the associative memory which makes the data memorize beforehand according to data is specified, and the technique which shortens the time amount which retrieval

and storage take by this is indicated.
[0006]
[Problem(s) to be Solved by the Invention] By the way, in the system using two or more associative memories, two or more associative memories used for the system are classified into plurality, and there is a case where he wants to access for every classification. However, although the method indicated by above-mentioned JP,3-52160,B is suitable for dealing with it in two or more associative memories by which cascade connection was carried out as if it was one associative memory with big memory space, it cannot access the associative memory of these plurality for every classification.
[0007] Moreover, although the associative memory which it had can be independently accessed with the technique proposed by above-mentioned JP,6-251589,B, since it is dependent on data, assignment of the associative memory accessed cannot access a desired associative memory freely. In view of the above-mentioned situation, this invention classifies the associative memory of these plurality into plurality, when it has two or more associative memories, and it aims at offering the associative memory system which can access the associative memory of these plurality freely for every classification.
[0008]
[Means for Solving the Problem] The associative memory system of this invention which attains the above-mentioned purpose is characterized by having the associative-memory control unit which changes into a chip enable condition the associative memory according to which it comes to classify into plurality two or more associative memories by which cascade connection may be carried out one by one, and the associative memory of these plurality, and which belongs to the classification of the request in the associative memory of these plurality alternatively for every classification.
[0009] It is desirable to have the propagation signal transformation section which the above-mentioned associative-memory control unit changes into the signal with which the signal which the associative memory of the latter part when cascade connection of those associative memories is carried out is made to spread was inputted, and this signal was separated from the above-mentioned associative memory for every above-mentioned classification, and which a latter associative memory is made to spread, and outputs towards the above-mentioned associative memory in the associative memory system of above-mentioned this invention here.
[0010] Or in the above-mentioned associative memory, when cascade connection of the above-mentioned associative memory is carried out, it has the classification separation circuit which separates logically the signal which a latter associative memory is made to spread for every above-mentioned classification, and you may come to carry out cascade connection of the above-mentioned associative memory one by one.
[0011]
[Function] Since the associative memory system of this invention is equipped with the associative-memory control unit which changes the associative memory belonging to the classification of the request in two or more associative memories into a chip enable condition, it can access the associative memory of these plurality freely for every classification. Here, when it does not connect with a cascade although the associative memory used for the associative memory system of this invention is equipped with the configuration by which cascade connection may be carried out one by one, instead an associative-memory control unit is equipped with the above-mentioned propagation signal transformation section, the associative memory system which the associative memory itself can moreover access for every classification, using the conventional associative memory to which cascade connection can be carried out one by one as it is is built.
[0012] Moreover, the associative memory system which can be accessed for every classification is built, without equipping an associative-memory control unit side with the above-mentioned propagation signal transformation section, when the associative memory used for the associative memory system of this invention builds in the above-mentioned classification separation circuit.
[0013]
[Example] Hereafter, the example of this invention is explained. Drawing 1 and drawing 2 are each in the 1st example of the associative memory system of this invention, an associative-memory control device, and the block diagram of an associative memory. As shown in drawing 2 , n associative memories 201-20n shall be used for the associative memory system shown here, and associative-memory 20 m1+m2+1-20 n after Classification B and it shall be classified [associative-memory 20 1-20 m1 / m1 piece] into Classification C for Classification A and associative-memory 20 m1+1-20 m1+m2 [m2 piece].
[0014] each -- read/write signal R/W_ for making read-out of the writing of the chip enable signals CE1-CEn

for putting each associative memory on an active condition, the search signal SEARCH which orders it to search to each associative memory, and the data to each associative memory, and the data from each associative memory perform and output enable signal OE_, and address signal ADDRESS that specifies the address inside each associative memory are inputted into associative-memory 20 1-20 n. Moreover, from each associative memory, the empty signal 1 - n showing the empty memory area where effective data are not stored in coincidence signal 1-n which shows that coincidence is detected by the associative memory by retrieval, and its associative memory existing are outputted. Moreover, from each associative memory, data DAT A which read data DAT A is outputted and should be written in each associative memory is inputted. Furthermore, when these associative memories are connected to a cascade, the empty external signal 1 which connect with a coincidence external signal 1-n [which shows whether it shifted and coincidence was detected by that associative memory linked to an upper case side], and upper case side shows whether shifts and has an opening in the memory area of that associative memory - n are inputted into each associative memory. When cascade connection is carried out, a coincidence signal linked to an upper case side [whether it shifted and coincidence was detected by that associative memory or its own associative memory, and] Or it becomes the signal with which either of the associative memory by the side of an upper case shows whether coincidence was detected from itself including itself. An empty signal also turns into a signal as for which connect with an upper case side shows similarly whether shifts and has an opening in that associative memory or its own associative memory, or there is not any opening in all of the associative memory by the side of an upper case rather than itself including itself.

[0015] The associative-memory control device 10 shown in drawing 1 is equipped with the associative-memory selection table 11 for coincidence signals, the associative-memory selection table 12 for empty signals, and the classification decoder 13. Each coincidence signal 1 of n associative memories shown in drawing 2 - n are inputted into the associative-memory selection table 11 for coincidence signals, and coincidence external signal 1-n and coincidence, or a signal is outputted to it.

[0016] Drawing 3 is drawing showing the contents of the associative-memory selection table 11 for coincidence signals shown in drawing 1 with a block. The contents of the classification A which consists of an m1 piece associative memory are shown here. any of coincidence signal 1-m1 -- although -- when 'L' level which shows that there was no coincidence is suited, while generating and outputting coincidence external signal 1-m1 of 'L' level altogether, on the associative-memory selection table 11 for coincidence signals, the coincidence of associative-memory 20 'L' level which shows that coincidence was not detected in any of 1 1-20m, or a signal is outputted.

[0017] Moreover, when either suits the coincidence signal 1 - 'H' level among m1, as shown in drawing 3 , [which shows that there was coincidence] The coincidence of 'H' level or the signal which shows that the coincidence external signal of 'H' level was outputted when there was no coincidence rather than itself at an upper case side and there was coincidence by the upper case side rather than itself, and there was coincidence by either with this is outputted. ['L' level and]

[0018] thus, coincidence external signal 1-m1 generated on the associative-memory selection table 11 for coincidence signals belongs to the classification A shown in drawing 2 , respectively -- each -- it is transmitted to associative-memory 20 1-20 m1. The same is said of Classifications B and C. The same is said of the associative-memory selection table 12 for empty signals shown in drawing 1 , and each empty signal 1 of n associative memories shown in drawing 2 - n are inputted into this associative-memory selection table 12 for empty signals, and the signal of the same logic as the associative-memory selection table 11 for coincidence signals shown in drawing 3 is outputted to it according to the logic ('H' level: with [it is vacant, and / be and] no 'L' level:opening) of those empty signals 1 - n. It is transmitted to each [which was generated on this associative-memory selection table 12 for empty signals / which shows an external signal 1 - n to drawing 2 by being vacant, respectively] associative memory 20_1 - 20_n.

[0019] The classification decoder 3 shown in drawing 1 inputs the chip enable signal CE, a classification selection signal, and an associative-memory number selection signal, and generates the chip enable signals CE1-CEn for every associative memory. The chip enable signal CE is a signal inputted when it is going to perform data writing to one or two or more associative memories which are specified with a classification selection signal and an associative-memory number selection signal, or data readout from them.

[0020] The classification selection signal consists of 2 bits here, and Classification A, Classification B, and Classification C are specified by '00', '01', and '10', respectively. When this classification selection signal is '11', an associative-memory number selection signal becomes effective. The associative-memory number

selection signal consists of 4 bits here, and an associative memory 20_1, an associative memory 20_2, --, an associative memory 20_15 are specified according to '0000', '0001', --, '1110'. However, the number n of the associative memory shown in drawing 2 here carries out to 15 or less. When an associative-memory number selection signal is '1111', all associative memories are specified.

[0021] When an example is given and a classification selection signal is '00', associative-memory 20_1-20_m1 [m1 piece] which belongs to Classification A regardless of an associative-memory number selection signal is specified. When a classification selection signal is '11' and an associative-memory number selection signal is '0000', Only an associative memory 20_1 is specified, a classification selection signal is '11', and when an associative-memory number selection signal is '1111', all the associative memories 20_1 - 20_n are specified.

[0022] At the classification decoder shown in drawing 1 , the chip enable signal (one or plurality of the chip enable signals CE1-CEn) of an associative memory is started on 'H' level showing chip enable based on the above-mentioned logic to the timing of the standup of enable signal CE. These chip enable signals CE1-CEn will be in the condition that the associative memory into which it was inputted into each associative memory 20_1 shown in drawing 2 - 20_n, respectively, and the signal of 'H' level was inputted as a chip enable signal is active.

[0023] Drawing 4 is the ** type circuit diagram showing the internal configuration of each associative memory shown in drawing 2 . In addition, only the part required for the following explanation is illustrated here, and the whole circuit is not shown. The associative memory cell array 21 in the associative memory 20 shown in this drawing 4 stores each data corresponding to each address, and it is constituted so that R/W and data retrieval of data can be performed. Moreover, a selector 22 writes the data which read data from the associative memory cell array, and outputted outside according to the control signal from the gates 31 and 32, or were inputted from the outside in the associative memory cell array 21.

[0024] The whole coincidence detector 23 is a circuit which coincidence was detected in one memory area of this associative memory 20, or ('H' level) coincidence was not detected in this associative memory 20, or ('L' level) is outputted, is the coincidence signal of each coincidence lines 114a, 114b, --, 114k shown in drawing 10 , or is generated by the operation.

[0025] Moreover, the whole opening detector 24 is a circuit which it is in the empty condition that effective data are not stored, or ('H' level) is stored in data effective in all the memory areas of this associative memory 20, or ('L' level) one memory area of this associative memory 20 outputs. If coincidence is detected in the whole coincidence detector 23, the signal showing the coincidence of 'H' level will be outputted towards the associative-memory control unit shown in drawing 1 via a gate circuit 25. Moreover, even if the signal of 'L' level which shows that coincidence was not detected by this associative memory 20 from the whole coincidence detector 23 is outputted, when a coincidence external signal is in 'H' level which shows that coincidence was detected by the associative memory by the side of an upper case, from the gate 25, the coincidence signal of 'H' level is outputted too. Namely, as for the signal of 'H' level being outputted from the gate 25, as for that coincidence was detected by the associative memory of either a oneself side and an upper case side, and the signal of 'L' level being outputted from the gate 25, any associative memory by the side of itself and an upper case means that coincidence was not detected.

[0026] Moreover, although the chip enable signal CE is inputted into an associative memory 20 The chip enable signal CE showing chip enable of 'H' level By gate circuits 27-29, a coincidence external signal is 'L' level (coincidence is detected for neither of the associative memories by the side of an upper case). And when the signal of 'H' level which shows that coincidence was detected by its own associative memory 20 is outputted, internal chip enable (interior CE) serves as 'H' level from whole its own associative-memory 20 coincidence detector 23. Or Interior CE serves as 'H' level, when the signal of 'H' level which an empty external signal is 'L' level (there is no opening in any associative memory by the side of an upper case), and shows that an opening is in its own associative memory 20 by gate circuits 28, 29, and 30 from the empty its own associative-memory 20 whole detector 24 is outputted. That is, Interior CE serves as 'H' level, in response to the fact that the chip enable signal CE was set to 'H' level when the priority of 'coincidence' exists in itself, or when 'empty' priority exists.

[0027] A gate circuit 31 has Interior CE in 'H' level, and if read/write signal R/W_ changes to 'L' level when output enable signal OE_ is in 'H' level further, it will output the control signal of 'H' level which directs writing to a selector 22. Moreover, a gate circuit 32 has Interior CE in 'H' level, and if an output enable signal changes to 'L' level when read/write signal R/W_ is in 'H' level further, it will output the signal of 'H' level

which directs read-out to a selector 22.
[0028] Drawing 5 is the timing chart of read-out of the associative memory system explained with reference to drawing 1 - drawing 4 . Here, a classification selection signal '00' is inputted into the associative-memory control device 10 first shown in drawing 1 , and the chip enable signal CE of 'H' level is inputted. Then, the chip enable signals CE1-CEm1 are outputted towards the m1 piece associative memory 20_1 belonging to Classification A (refer to drawing 2), 20_2, --, 20_m1. Then, the search signal SEARCH is inputted into each associative memory 20_1 - 20_n. Then, retrieval is performed about the m1 piece associative memory 20_1 belonging to Classification A, 20_2, --, 20_m1. Here, it considers as the m1 piece associative memory 20_1 belonging to Classification A, 20_2, --, two associative memories 20_1 and the thing by which every one coincidence was detected by 20_2 the upper case side of 20_m1 by this retrieval.
[0029] The m1 piece associative memory 20_1 belonging to the classification A shown in drawing 2 , 20_2, --, each coincidence signal 'H, H, L, --, L' of 20_m1 It is inputted into the associative-memory selection table 11 for coincidence signals of the associative-memory control device 10 shown in drawing 1 , and thereby, coincidence external signal 1-m1 of 'L, H, --, H' is generated, and it is inputted into each associative memory 20_1 of Classification A, 20_2, --, 20_m1. Two associative memories 20_1, the coincidence signals 1 and 2 about 20_2, and the coincidence external signals 1 and 2 are shown in drawing 5 the upper case side.
[0030] If output enable signal OE_ is changed to 'L' level in the condition, maintaining read/write signal R/W_ at 'H' level, read-out will be performed about the associative memory 20_1 of the maximum upper case where 'H' level and a coincidence external signal have a coincidence signal in 'L' level. If the memory area which is a memory area where coincidence was detected and is not read to an associative memory 20_1 by this read-out is lost, the coincidence signal of an associative memory 20_1 will change to 'L' level. Since the coincidence external signal 2 corresponding to an associative memory 20_2 changes to 'L' level and the coincidence signal 2 of the associative memory 20_2 has it in 'H' level in response to it, if output enable signal OE_ changes to 'L' level next, data will be shortly read from an associative memory 20_2.
[0031] Drawing 6 is the timing chart of the data writing of the associative memory system explained with reference to drawing 1 - drawing 4 . If it refers to the same sequence as read-out explained with reference to drawing 5 , it will be vacant in an associative memory with an opening, and a signal will be generated and outputted. Here, it considers as the m1 piece associative memory 20_1 belonging to Classification A, 20_2, --, two associative memories 20_1 by the side of the upper case of 20_m1 and the thing by which one opening was detected at a time by 20_2 like the case of drawing 5 .
[0032] The m1 piece associative memory 20_1 belonging to the classification A shown in drawing 2 , 20_2, --, each empty signal 'H, H, L, --, L' of 20_m1 It is inputted into the associative-memory selection table 12 for empty signals of the associative-memory control device 10 shown in drawing 1 , and thereby, empty external signal 1-m1 of 'L, H, --, H' is generated, and it is inputted into each associative memory 20_1 of Classification A, 20_2, --, 20_m1. In drawing 6 , it is [about two associative memories 20_1 and 20_2] vacant an upper case side, and signals 1 and 2 and the empty external signals 1 and 2 are shown.
[0033] If read/write signal R/W_ is changed to 'L' level, maintaining output enable signal OE_ at 'H' level in the condition, data writing will be performed about the associative memory 20_1 of the maximum upper case where 'H' level and an empty external signal have an empty signal in 'L' level. If a free area is lost to an associative memory 20_1 and the coincidence signal of an associative memory 20_1 changes with these data writing to 'L' level Since the empty external signal 2 corresponding to an associative memory 20_2 changes to 'L' level and the empty signal 2 of the associative memory 20_2 has it in 'H' level in response to it, If read/write signal R/W_ changes to 'L' level next, data will be shortly written in an associative memory 20_2.
[0034] Drawing 7 and drawing 8 are each in the 2nd example of the associative memory system of this invention, an associative-memory control device, and the block diagram of an associative memory. It has only the part corresponding to the classification decoder B of the associative-memory control device 10 which shows these five associative memories 50_1, 50_2, --, the associative-memory control device 40 that 50_5 shows to drawing 7 to drawing 1 . however, the associative-memory parameter which shows the associative-memory control unit 40 shown in drawing 7 to drawing 1 is inputted -- as -- it is not constituted. That is, the associative-memory control unit 40 shown in drawing 7 is the thing of the single function in which the chip enable signal CE of 'H' level is outputted towards the associative memory which inputs a classification selection signal and belongs to the classification according to the classification selection signal.
[0035] Moreover, as shown in drawing 8 , it has five associative memories 50_1, 50_2, --, 50_5, and cascade connection of this 2nd example is carried out one by one. Here, two consider as these five associative

memories 50_1, 50_2, --, the thing from which one of Classification B and the bottoms is divided into Classification C for Classification A and the following two an upper case side among 50_5.
[0036] Drawing 9 is the ** type circuit diagram showing the internal configuration of each associative memory of drawing 8 . Difference with the associative memory in the 1st example shown in drawing 4 is explained. The classification head register 33 and gate circuits 34 and 35 are added to the associative memory 20 shown in the associative memory 50 shown in drawing 9 at drawing 4 . In not being the flag of 'H' level, and the head of oneself a classification in the case of the head (the associative memory 50_1 shown in drawing 8 , 50_3, 50_5) of oneself a classification (the associative memory 50_2, 50_4 which are shown in drawing 8), the flag of 'L' level is stored in the classification head register 33. Therefore, when this associative memory 50 is in the head of a classification, the coincidence external signal of 'H' level which shows that there was coincidence by the upper case side is prevented in a gate circuit 34, and is treated as a thing without coincidence by the upper case side. Moreover, the same is said of an empty external signal, and the empty external signal of 'H' level which shows that an opening is in an upper case side is prevented in a gate circuit 35, and is treated as a thing without an opening by the upper case side. Namely, the coincidence signal and the empty signal which the associative memory of the latter part by which cascade connection was carried out is made to spread are logically separated for every classification.
[0037] Thus, access which became independent for every classification is attained by separating logically and making only the associative memory belonging to a desired classification into chip enable with the associative-memory control device 40 shown in drawing 7 .
[0038]
[Effect of the Invention] As explained above, according to this invention, in the associative memory system equipped with two or more associative memories, the associative memory of these plurality is classified into plurality, and the associative memory of these plurality can be freely accessed for every classification.

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OPERATION

[Function] Since the associative memory system of this invention is equipped with the associative-memory control unit which changes the associative memory belonging to the classification of the request in two or more associative memories into a chip enable condition, it can access the associative memory of these plurality freely for every classification. Here, when it does not connect with a cascade although the associative memory used for the associative memory system of this invention is equipped with the configuration by which cascade connection may be carried out one by one, instead an associative-memory control unit is equipped with the above-mentioned propagation signal transformation section, the associative memory system which the associative memory itself can moreover access for every classification, using the conventional associative memory to which cascade connection can be carried out one by one as it is is built. [0012] Moreover, the associative memory system which can be accessed for every classification is built, without equipping an associative-memory control unit side with the above-mentioned propagation signal transformation section, when the associative memory used for the associative memory system of this invention builds in the above-mentioned classification separation circuit.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] Hereafter, the example of this invention is explained. Drawing 1 and drawing 2 are each in the 1st example of the associative memory system of this invention, an associative-memory control device, and the block diagram of an associative memory. As shown in drawing 2 , n associative memories 201-20n shall be used for the associative memory system shown here, and associative-memory 20 m1+m2+1-20 n after Classification B and it shall be classified [associative-memory 20 1-20 m1 / m1 piece] into Classification C for Classification A and associative-memory 20 m1+1-20 m1+m2 [m2 piece].
[0014] each -- read/write signal R/W_ for making read-out of the writing of the chip enable signals CE1-CEn for putting each associative memory on an active condition, the search signal SEARCH which orders it to search to each associative memory, and the data to each associative memory, and the data from each associative memory perform and output enable signal OE_, and address signal ADDRESS that specifies the address inside each associative memory are inputted into associative-memory 20 1-20 n. Moreover, from each associative memory, the empty signal 1 - n showing the empty memory area where effective data are not stored in coincidence signal 1-n which shows that coincidence is detected by the associative memory by retrieval, and its associative memory existing are outputted. Moreover, from each associative memory, data DAT A which read data DAT A is outputted and should be written in each associative memory is inputted. Furthermore, when these associative memories are connected to a cascade, the empty external signal 1 which connect with a coincidence external signal 1-n [which shows whether it shifted and coincidence was detected by that associative memory linked to an upper case side], and upper case side shows whether shifts and has an opening in the memory area of that associative memory - n are inputted into each associative memory. When cascade connection is carried out, a coincidence signal linked to an upper case side [whether it shifted and coincidence was detected by that associative memory or its own associative memory, and] Or it becomes the signal with which either of the associative memory by the side of an upper case shows whether coincidence was detected from itself including itself. An empty signal also turns into a signal as for which connect with an upper case side shows similarly whether shifts and has an opening in that associative memory or its own associative memory, or there is not any opening in all of the associative memory by the side of an upper case rather than itself including itself.
[0015] The associative-memory control device 10 shown in drawing 1 is equipped with the associative-memory selection table 11 for coincidence signals, the associative-memory selection table 12 for empty signals, and the classification decoder 13. Each coincidence signal 1 of n associative memories shown in drawing 2 - n are inputted into the associative-memory selection table 11 for coincidence signals, and coincidence external signal 1-n and coincidence, or a signal is outputted to it.
[0016] Drawing 3 is drawing showing the contents of the associative-memory selection table 11 for coincidence signals shown in drawing 1 with a block. The contents of the classification A which consists of an m1 piece associative memory are shown here. any of coincidence signal 1-m1 -- although -- when 'L' level which shows that there was no coincidence is suited, while generating and outputting coincidence external signal 1-m1 of 'L' level altogether, on the associative-memory selection table 11 for coincidence signals, the coincidence of associative-memory 20 'L' level which shows that coincidence was not detected in any of 1 1-20m, or a signal is outputted.
[0017] Moreover, when either suits the coincidence signal 1 - 'H' level among m1, as shown in drawing 3 , [which shows that there was coincidence] The coincidence of 'H' level or the signal which shows that the coincidence external signal of 'H' level was outputted when there was no coincidence rather than itself at an upper case side and there was coincidence by the upper case side rather than itself, and there was coincidence

by either with this is outputted. ['L' level and]
[0018] thus, coincidence external signal 1-m1 generated on the associative-memory selection table 11 for coincidence signals belongs to the classification A shown in drawing 2 , respectively -- each -- it is transmitted to associative-memory 20 1-20 m1. The same is said of Classifications B and C. The same is said of the associative-memory selection table 12 for empty signals shown in drawing 1 , and each empty signal 1 of n associative memories shown in drawing 2 - n are inputted into this associative-memory selection table 12 for empty signals, and the signal of the same logic as the associative-memory selection table 11 for coincidence signals shown in drawing 3 is outputted to it according to the logic ('H' level: with [it is vacant, and / be and] no 'L' level:opening) of those empty signals 1 - n. It is transmitted to each [which was generated on this associative-memory selection table 12 for empty signals / which shows an external signal 1 - n to drawing 2 by being vacant, respectively] associative memory 20_1 - 20_n.
[0019] The classification decoder 3 shown in drawing 1 inputs the chip enable signal CE, a classification selection signal, and an associative-memory number selection signal, and generates the chip enable signals CE1-CEn for every associative memory. The chip enable signal CE is a signal inputted when it is going to perform data writing to one or two or more associative memories which are specified with a classification selection signal and an associative-memory number selection signal, or data readout from them.
[0020] The classification selection signal consists of 2 bits here, and Classification A, Classification B, and Classification C are specified by '00', '01', and '10', respectively. When this classification selection signal is '11', an associative-memory number selection signal becomes effective. The associative-memory number selection signal consists of 4 bits here, and an associative memory 20_1, an associative memory 20_2, --, an associative memory 20_15 are specified according to '0000', '0001', --, '1110'. However, the number n of the associative memory shown in drawing 2 here carries out to 15 or less. When an associative-memory number selection signal is '1111', all associative memories are specified.
[0021] When an example is given and a classification selection signal is '00', associative-memory 20_1-20_m1 [m1 piece] which belongs to Classification A regardless of an associative-memory number selection signal is specified. When a classification selection signal is '11' and an associative-memory number selection signal is '0000', Only an associative memory 20_1 is specified, a classification selection signal is '11', and when an associative-memory number selection signal is '1111', all the associative memories 20_1 - 20_n are specified.
[0022] At the classification decoder shown in drawing 1 , the chip enable signal (one or plurality of the chip enable signals CE1-CEn) of an associative memory is started on 'H' level showing chip enable based on the above-mentioned logic to the timing of the standup of enable signal CE. These chip enable signals CE1-CEn will be in the condition that the associative memory into which it was inputted into each associative memory 20_1 shown in drawing 2 - 20_n, respectively, and the signal of 'H' level was inputted as a chip enable signal is active.
[0023] Drawing 4 is the ** type circuit diagram showing the internal configuration of each associative memory shown in drawing 2 . In addition, only the part required for the following explanation is illustrated here, and the whole circuit is not shown. The associative memory cell array 21 in the associative memory 20 shown in this drawing 4 stores each data corresponding to each address, and it is constituted so that R/W and data retrieval of data can be performed. Moreover, a selector 22 writes the data which read data from the associative memory cell array, and outputted outside according to the control signal from the gates 31 and 32, or were inputted from the outside in the associative memory cell array 21.
[0024] The whole coincidence detector 23 is a circuit which coincidence was detected in one memory area of this associative memory 20, or ('H' level) coincidence was not detected in this associative memory 20, or ('L' level) is outputted, is the coincidence signal of each coincidence lines 114a, 114b, --, 114k shown in drawing 10 , or is generated by the operation.
[0025] Moreover, the whole opening detector 24 is a circuit which it is in the empty condition that effective data are not stored, or ('H' level) is stored in data effective in all the memory areas of this associative memory 20, or ('L' level) one memory area of this associative memory 20 outputs. If coincidence is detected in the whole coincidence detector 23, the signal showing the coincidence of 'H' level will be outputted towards the associative-memory control unit shown in drawing 1 via a gate circuit 25. Moreover, even if the signal of 'L' level which shows that coincidence was not detected by this associative memory 20 from the whole coincidence detector 23 is outputted, when a coincidence external signal is in 'H' level which shows that coincidence was detected by the associative memory by the side of an upper case, from the gate 25, the

coincidence signal of 'H' level is outputted too. Namely, as for the signal of 'H' level being outputted from the gate 25, as for that coincidence was detected by the associative memory of either a oneself side and an upper case side, and the signal of 'L' level being outputted from the gate 25, any associative memory by the side of itself and an upper case means that coincidence was not detected.

[0026] Moreover, although the chip enable signal CE is inputted into an associative memory 20 The chip enable signal CE showing chip enable of 'H' level By gate circuits 27-29, a coincidence external signal is 'L' level (coincidence is detected for neither of the associative memories by the side of an upper case). And when the signal of 'H' level which shows that coincidence was detected by its own associative memory 20 is outputted, internal chip enable (interior CE) serves as 'H' level from whole its own associative-memory 20 coincidence detector 23. Or Interior CE serves as 'H' level, when the signal of 'H' level which an empty external signal is 'L' level (there is no opening in any associative memory by the side of an upper case), and shows that an opening is in its own associative memory 20 by gate circuits 28, 29, and 30 from the empty its own associative-memory 20 whole detector 24 is outputted. That is, Interior CE serves as 'H' level, in response to the fact that the chip enable signal CE was set to 'H' level when the priority of 'coincidence' exists in itself, or when 'empty' priority exists.

[0027] A gate circuit 31 has Interior CE in 'H' level, and if read/write signal R/W_ changes to 'L' level when output enable signal OE_ is in 'H' level further, it will output the control signal of 'H' level which directs writing to a selector 22. Moreover, a gate circuit 32 has Interior CE in 'H' level, and if an output enable signal changes to 'L' level when read/write signal R/W_ is in 'H' level further, it will output the signal of 'H' level which directs read-out to a selector 22.

[0028] Drawing 5 is the timing chart of read-out of the associative memory system explained with reference to drawing 1 - drawing 4 . Here, a classification selection signal '00' is inputted into the associative-memory control device 10 first shown in drawing 1 , and the chip enable signal CE of 'H' level is inputted. Then, the chip enable signals CE1-CEm1 are outputted towards the m1 piece associative memory 20_1 belonging to Classification A (refer to drawing 2), 20_2, --, 20_m1. Then, the search signal SEARCH is inputted into each associative memory 20_1 - 20_n. Then, retrieval is performed about the m1 piece associative memory 20_1 belonging to Classification A, 20_2, --, 20_m1. Here, it considers as the m1 piece associative memory 20_1 belonging to Classification A, 20_2, --, two associative memories 20_1 and the thing by which every one coincidence was detected by 20_2 the upper case side of 20_m1 by this retrieval.

[0029] The m1 piece associative memory 20_1 belonging to the classification A shown in drawing 2 , 20_2, --, each coincidence signal 'H, H, L, --, L' of 20_m1 It is inputted into the associative-memory selection table 11 for coincidence signals of the associative-memory control device 10 shown in drawing 1 , and thereby, coincidence external signal 1-m1 of 'L, H, --, H' is generated, and it is inputted into each associative memory 20_1 of Classification A, 20_2, --, 20_m1. Two associative memories 20_1, the coincidence signals 1 and 2 about 20_2, and the coincidence external signals 1 and 2 are shown in drawing 5 the upper case side.

[0030] If output enable signal OE_ is changed to 'L' level in the condition, maintaining read/write signal R/W_ at 'H' level, read-out will be performed about the associative memory 20_1 of the maximum upper case where 'H' level and a coincidence external signal have a coincidence signal in 'L' level. If the memory area which is a memory area where coincidence was detected and is not read to an associative memory 20_1 by this read-out is lost, the coincidence signal of an associative memory 20_1 will change to 'L' level. Since the coincidence external signal 2 corresponding to an associative memory 20_2 changes to 'L' level and the coincidence signal 2 of the associative memory 20_2 has it in 'H' level in response to it, if output enable signal OE_ changes to 'L' level next, data will be shortly read from an associative memory 20_2.

[0031] Drawing 6 is the timing chart of the data writing of the associative memory system explained with reference to drawing 1 - drawing 4 . If it refers to the same sequence as read-out explained with reference to drawing 5 , it will be vacant in an associative memory with an opening, and a signal will be generated and outputted. Here, it considers as the m1 piece associative memory 20_1 belonging to Classification A, 20_2, --, two associative memories 20_1 by the side of the upper case of 20_m1 and the thing by which one opening was detected at a time by 20_2 like the case of drawing 5 .

[0032] The m1 piece associative memory 20_1 belonging to the classification A shown in drawing 2 , 20_2, --, each empty signal 'H, H, L, --, L' of 20_m1 It is inputted into the associative-memory selection table 12 for empty signals of the associative-memory control device 10 shown in drawing 1 , and thereby, empty external signal 1-m1 of 'L, H, --, H' is generated, and it is inputted into each associative memory 20_1 of Classification A, 20_2, --, 20_m1. In drawing 6 , it is [about two associative memories 20_1 and 20_2] vacant an upper

case side, and signals 1 and 2 and the empty external signals 1 and 2 are shown.
[0033] If read/write signal R/W_ is changed to 'L' level, maintaining output enable signal OE_ at 'H' level in the condition, data writing will be performed about the associative memory 20_1 of the maximum upper case where 'H' level and an empty external signal have an empty signal in 'L' level. If a free area is lost to an associative memory 20_1 and the coincidence signal of an associative memory 20_1 changes with these data writing to 'L' level Since the empty external signal 2 corresponding to an associative memory 20_2 changes to 'L' level and the empty signal 2 of the associative memory 20_2 has it in 'H' level in response to it, If read/write signal R/W_ changes to 'L' level next, data will be shortly written in an associative memory 20_2.
[0034] Drawing 7 and drawing 8 are each in the 2nd example of the associative memory system of this invention, an associative-memory control device, and the block diagram of an associative memory. It has only the part corresponding to the classification decoder B of the associative-memory control device 10 which shows these five associative memories 50_1, 50_2, --, the associative-memory control device 40 that 50_5 shows to drawing 7 to drawing 1 . however, the associative-memory parameter which shows the associative-memory control unit 40 shown in drawing 7 to drawing 1 is inputted -- as -- it is not constituted. That is, the associative-memory control unit 40 shown in drawing 7 is the thing of the single function in which the chip enable signal CE of 'H' level is outputted towards the associative memory which inputs a classification selection signal and belongs to the classification according to the classification selection signal.
[0035] Moreover, as shown in drawing 8 , it has five associative memories 50_1, 50_2, --, 50_5, and cascade connection of this 2nd example is carried out one by one. Here, two consider as these five associative memories 50_1, 50_2, --, the thing from which one of Classification B and the bottoms is divided into Classification C for Classification A and the following two an upper case side among 50_5.
[0036] Drawing 9 is the ** type circuit diagram showing the internal configuration of each associative memory of drawing 8 . Difference with the associative memory in the 1st example shown in drawing 4 is explained. The classification head register 33 and gate circuits 34 and 35 are added to the associative memory 20 shown in the associative memory 50 shown in drawing 9 at drawing 4 . In not being the flag of 'H' level, and the head of oneself a classification in the case of the head (the associative memory 50_1 shown in drawing 8 , 50_3, 50_5) of oneself a classification (the associative memory 50_2, 50_4 which are shown in drawing 8), the flag of 'L' level is stored in the classification head register 33. Therefore, when this associative memory 50 is in the head of a classification, the coincidence external signal of 'H' level which shows that there was coincidence by the upper case side is prevented in a gate circuit 34, and is treated as a thing without coincidence by the upper case side. Moreover, the same is said of an empty external signal, and the empty external signal of 'H' level which shows that an opening is in an upper case side is prevented in a gate circuit 35, and is treated as a thing without an opening by the upper case side. Namely, the coincidence signal and the empty signal which the associative memory of the latter part by which cascade connection was carried out is made to spread are logically separated for every classification.
[0037] Thus, access which became independent for every classification is attained by separating logically and making only the associative memory belonging to a desired classification into chip enable with the associative-memory control device 40 shown in drawing 7 .

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The associative memory system characterized by having the associative-memory control unit which changes into a chip enable condition two or more associative memories by which cascade connection may be carried out one by one, and the associative memory according to which it comes to classify said two or more associative memories into plurality, and which belongs to the classification of the request in said two or more associative memories alternatively for every classification.
[Claim 2] The associative memory system according to claim 1 characterized by having the propagation signal transformation section which said associative-memory control unit changes into the signal with which the signal which the associative memory of the latter part when cascade connection of this associative memory is carried out is made to spread was inputted, and this signal was separated from said associative memory for said every classification, and which a latter associative memory is made to spread, and outputs towards said associative memory.
[Claim 3] The associative memory system characterized by it having the classification separation circuit which separates logically the signal which a latter associative memory is made to spread for said every classification when cascade connection of said associative memory is carried out, and coming to carry out cascade connection of said associative memory one by one.

[Translation done.]

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2.**** shows the word which can not be translated.
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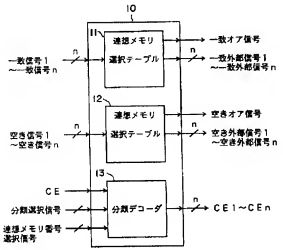
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the associative-memory control device in the 1st example of the associative memory system of this invention.
[Drawing 2] It is the block diagram of the associative memory in the 1st example of the associative memory system of this invention.
[Drawing 3] It is drawing showing the contents of the associative-memory selection table for coincidence signals.
[Drawing 4] It is the ** type circuit diagram showing the internal configuration of an associative memory.
[Drawing 5] It is the timing chart of read-out of an associative memory system.
[Drawing 6] It is the timing chart of the data writing of an associative memory system.
[Drawing 7] It is the block diagram of the associative-memory control device in the 2nd example of the associative memory system of this invention.
[Drawing 8] It is the block diagram of the associative memory in the 2nd example of the associative memory system of this invention.
[Drawing 9] It is the ** type circuit diagram showing the internal configuration of each associative memory of drawing 8 .
[Drawing 10] It is a circuit block diagram showing an example of an associative memory.
[Description of Notations]
10 40 Associative-memory control unit
11 12 Associative-memory selection table
13 Classification Decoder
20, 20_1, --, 20_m1, --, 20_n, 50, 50_1, 50_2, --, 50_5 Associative memory

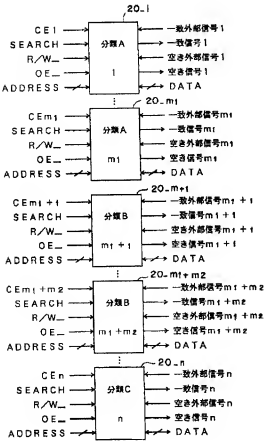
[Translation done.]

Drawing selection drawing 1



[Translation done.]

Drawing selection drawing 2



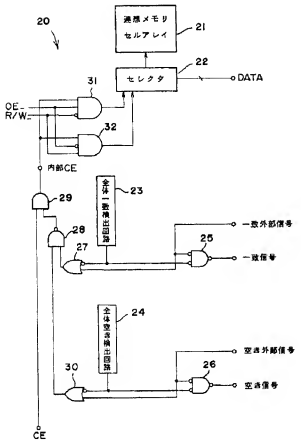
[Translation done.]

Drawing selection drawing 3

一致信号						一致外部信号					一致オア信号
1	2	3	4	…	m1	1	2	3	4	…	m1	
L	L	L	L	…	L	L	L	L	L	…	L	L
H	L	L	L	…	L	L	H	H	H	…	H	H
L	H	L	L	…	L	L	L	H	H	…	H	H
		⋮						⋮				⋮
L	H	H	H	…	L	L	L	H	H	…	H	H
		⋮						⋮				⋮
H	H	H	H	…	H	L	H	H	H	…	H	H
H：一致あり L：一致なし						H：上段で一致あり L：上段で一致なし						H：全体で一致あり L：全体で一致なし

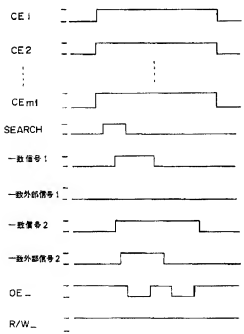
[Translation done.]

Drawing selection drawing 4



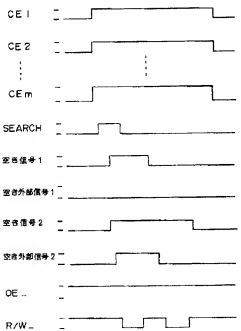
[Translation done.]

Drawing selection drawing 5



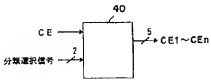
[Translation done.]

Drawing selection drawing 6



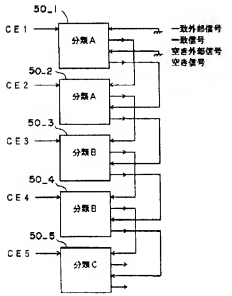
[Translation done.]

Drawing selection drawing 7



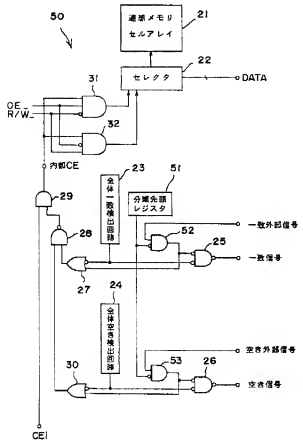
[Translation done.]

Drawing selection drawing 8



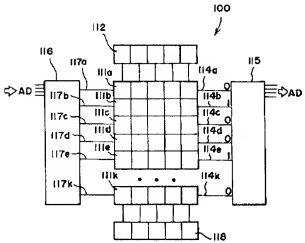
[Translation done.]

Drawing selection drawing 9



[Translation done.]

Drawing selection drawing 10



[Translation done.]